A HIGHLY RELIABLE 16 OUTPUT HIGH VOLTAGE NMOS/CMOS LOGIC IC WITH SHIELDED SOURCE STRUCTURE

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ABSTRACT

A high voltage MOS IC, which consists of 16 high voltage NMOS transistor array having 400 V, 0.5 A output characteristic and its control CMOS logic, was newly developed. High and low voltage NMOS transistors of the IC are equipped with shielded source structure to realize completely parasitic bipolar effect-free high voltage MOS ICs.

Practically, this IC successfully drove a plasma display panel at 200 V, 2 MHz without any parasitic effect and its high operation reliability was verified.

To examine high integration density possibility, parasitic bipolar effects due to the interferences between high and high voltage transistors, low and low voltage transistors, and high and low voltage transistors, were experimentally investigated. As a result, it was confirmed that the "shielded source structure" realizes high density high voltage MOS ICs.

INTRODUCTION

Recently, the cost and size reduction, and display area enlargement of flat display panels, such as PDP, ELD and dot matrix VFD, have been strongly demanded. Driver circuits for these display panels, necessarily have a lot of high voltage circuit outputs. Therefore, the monolithic IC equipped with high voltage transistors and their control logic circuits on the same chip, is essential to meet the above requirement. High voltage planar MOS ICs are thought to be most suited for such an IC, because of its isolation ease and high speed operation.[1]~[3]

However, negative resistance breakdown due to parasitic bipolar effect, is known to be observed in a high voltage planar NMOS transistor, a key device for high voltage MOS ICs.[4] Therefore, the high voltage transistor has a narrow ASO (Area of Safe Operation). To solve this problem, a high voltage MOS transistor with parasitic effect-free characteristic, was realized using the proposed "shielded source structure".[5][6]

The low voltage logic, for controlling the high voltage transistors, should be CMOS with low power dissipation and large noise immunity characteristic. However, since high resistivity substrate is used to realize high breakdown voltage for the high voltage MOS transistor, latch up phenomena in CMOS logic become easily to occur. Since the latch up is one of parasitic bipolar effect, the shielded source structure will be effective to suppress the latch up.

This paper describes, a newly developed, 16 output high voltage NMOS/CMOS logic IC without any parasitic effect. This is achieved by adopting shielded source structure. The possibility of realizing even higher integration density IC by using the shielded source structure is also discussed, based on experimental results.

DEVICE STRUCTURE

In the new IC, the shielded source structure, in which the high impurity density p^+ ground layer entirely covers n^+ source layer except for the MOS channel plane, is adopted in high voltage NMOS transistors and in low voltage NMOS transistors for CMOS logic, as shown in Fig. 1. Since p^+ ground layer potential is equal to that for the source (n^+), even if voltage drop at the substrate due to substrate current occurs, the source junction is not forward-biased. In consequence, the parasitic bipolar effect doesn't occur. These n^+ source layer and underlying p^+ ground layer are simply fabricated by As^+ and B^+ ion implantations through the same source mask windows in a self-aligned manner.

The IC is made up of 8 input-output buffer circuits, 16 blocks of serial-in/parallel-out shift register, latch, gate and buffer circuit and 16 output high voltage NMOS transistors (Fig. 2). The buffer circuit consisting of 4 stage inverters is designed to have 5 MHz driving capability for the high voltage transistor gate. The high voltage transistors are controlled by Output Enable (OE), Toggle (To) and Data (D in1 or D in2) input signals. The CMOS logic includes about 700 low voltage MOS transistors.

EXPERIMENTAL RESULTS

A photomicrograph of the IC is shown in Fig. 3. IC chip size is 6 mm x 6 mm. The IC electrical characteristics are shown in Table 1. High voltage NMOS transistors having 4 μm long, 10.2 mm wide MOS channel and 40 μm long offset gate, can flow 0.5 A drain current at 10 V gate bias, which is a high enough current level to drive a large display area dot matrix AC refresh PDP. The high voltage transistor shows about 400 V drain breakdown voltage in the 0 V to 15 V wide gate bias range without any negative resistance, according to pulse current-voltage measurement. This characteristic is still superior to that for 100-150 μm long offset gate conventional NMOS transistors. The conventional transistors have larger on-resistance and larger chip

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occupation area compared to that for the shielded source transistor. Therefore, this structure enables easily realizing high integration density MOS ICs. Drain current-voltage characteristics for the high voltage shielded source transistor are shown in Fig. 4.

CMOS logic with shielded source structure (about 4 μm gate length) operates at 2-30 V power supply voltage range and follows 9 MHz clock frequency at 10 V (Fig. 5) (5-6 MHz clock frequency will be large enough for about 2000 character AC refresh PDP to be driven). CMOS logic power consumption is 21 mW at 10 V, 5 MHz clock frequency, which is much less than the power consumption for an E/D MOS logic (over 100 mW).

If integration density increases further, there is a possibility that logic error operation due to a capacitive coupling noise pulse would occur. By using CMOS configuration in logic, stable logic operation is expected to be obtained due to its large noise margin. The other possibility is that the interferences between high and high voltage transistors, high and low voltage transistors, and low and low voltage transistors due to a substrate current, would occur. The substrate current will be caused by low and high voltage transistor's avalanche phenomena, p-n junction's (for example, drain junction for CMOS logic) forward-biasing resulting from capacitive coupling noise pulse and surge voltage.

For example, a large quantity of electrons injected into the substrate diffuse to a certain high voltage transistor and are likely to lead this transistor to negative resistance breakdown by causing the parasitic bipolar transistor to turn on. To investigate such a parasitic bipolar effect, the following experiment was made. In a high voltage transistor biased at a lower voltage than its breakdown voltage, electrons are injected from an adjacent high voltage transistor's drain junction into the substrate, by forward-biasing. These electrons enter into the transistor drain depletion layer and cause avalanche breakdown. As a result, a large quantity of holes are injected into the substrate and cause voltage drop at the substrate. According to the experiment, a conventional transistor showed parasitic bipolar action in low injection current in spite of at lower electric field than that of breakdown, whereas the shielded source transistor didn't show negative resistance breakdown, even at experimentally observable 450 mA injection current level.

Also, there is a possibility that latch up might occur in CMOS logic due to the substrate current. Since high voltage MOS IC uses high resistivity substrate, parasitic lateral npn transistor's base resistance, or the substrate resistance, is high, as mentioned previously. Therefore, when the substrate current causes enough voltage drop at the substrate resistance to make n-channel transistor source junction forward-bias, latch up occurs. In order to investigate such a parasitic bipolar effect, CMOS ability to withstand latch up was experimented upon. The conventional CMOS with 20 μm parasitic lateral npn transistor base (p^- substrate: $N_A = 6 \times 10^{14}$ cm^{-3}) width L_M, results in latch up phenomena, as shown in Fig. 6, at 6 mA parasitic vertical pnp transistor base (n-well region) injection current level, 10 V collector-emitter bias voltage. As compared with this characteristic, the CMOS with shielded source structure doesn't show latch up, even at 300-350 mA base injection current level. The reason is that current gain α_n for the parasitic npn transistor in the shielded source structure is less than 3×10^{-7}. These experimental investigations show that higher integration density IC will be realized.

The fabricated ICs in 28 pin ceramic packages were applied in a plasma display scan driver. The ICs successfully drove the panel at 200 V, 2 MHz without any parasitic effect and any logic operation error due to a capacitive coupling noise pulse (Fig. 7). As a result, in a practically usable high voltage IC, since parasitic bipolar action was effectively suppressed by using the shielded source structure, the high IC reliability was confirmed.

CONCLUSION

A 16 output high voltage NMOS/CMOS logic IC, designed for driving an AC refresh PDP, was developed using shielded source structure for its NMOS tansistors, to realize completely parasitic effect-free high voltage MOS ICs.

Practically, the IC succeeded in driving an AC refresh PDP and its high reliability was verified.

Parasitic effects due to the interferences between high and high voltage transistors, low and high voltage transistors, and low and low voltage transistors in this IC, were experimentally investigated.

These results indicate that much higher packing density, but still a parasitic effect-free high voltage NMOS/CMOS logic IC, will be realized using shielded source structure.

ACKNOWLEDGEMENT

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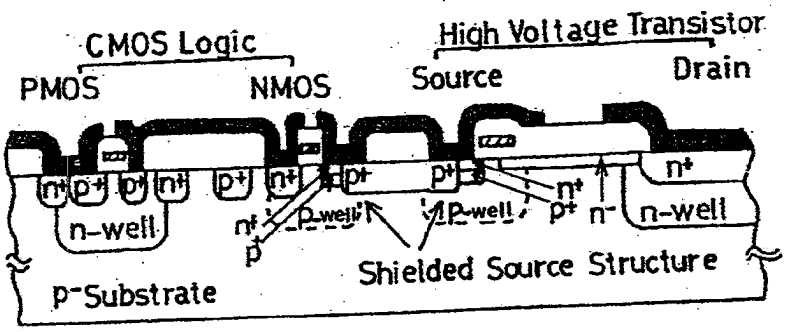

Fig.1 Cross sectional view of high voltage MOS IC with low voltage CMOS logic circuit. Both high and low voltage NMOS transistors have shielded source structure consisting of an upper n^+ source layer entirely shielded by a lower p^+ ground layer.

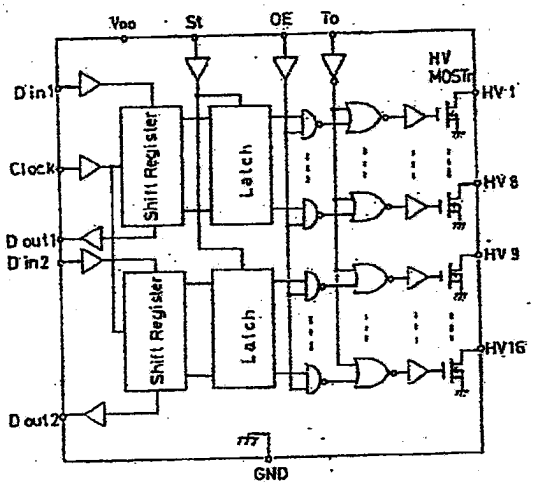

Fig.2 16 output high voltage MOS IC blockdiagram. Logic circuit is composed of serial-in and parallel-out shift registers, latches, gates and buffers.

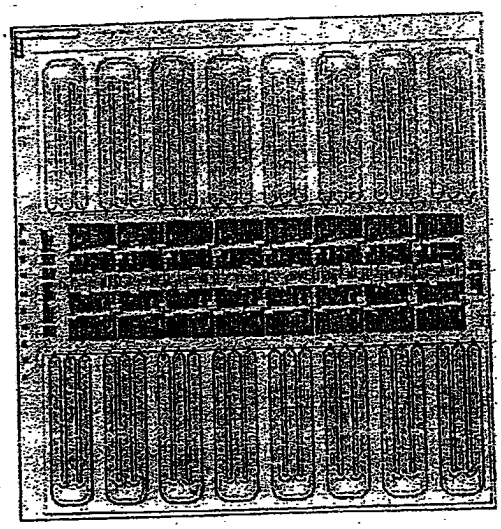

Fig.3 16 output high voltage MOS IC photomicrograph. Chip size is 6 mm x 6 mm.

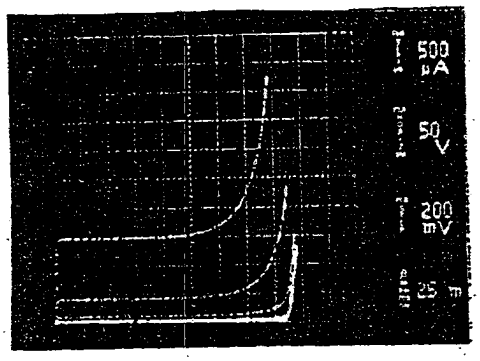

Fig.4 I-V characteristic for high voltage NMOS transistor with shielded source structure, which shows about 400 V drain breakdown voltage.

High Voltage MOS Tr	
BV_{DSS} (at I_D<100 μA)	400 V
Ron (at V_G=10 V)	30 Ω
I_{DS} (at V_G=10 V)	0.5 A
Low Voltage Logic Circuit	
f_{clock} max (at V_{DD}=10 V)	9 MHz
V_{DD}	2V~30 V
P_D (at V_{DD}=10V, f_{clock}=5MHz, C_L=15pF)	21 mw

Table 1 Typical 16 output high voltage MOS IC characteristics. CMOS logic circuit can operate in wide power supply voltage range. High voltage NMOS transistor doesn't show any parasitic bipolar effect for wide gate bias range from 0 V to 15 V.

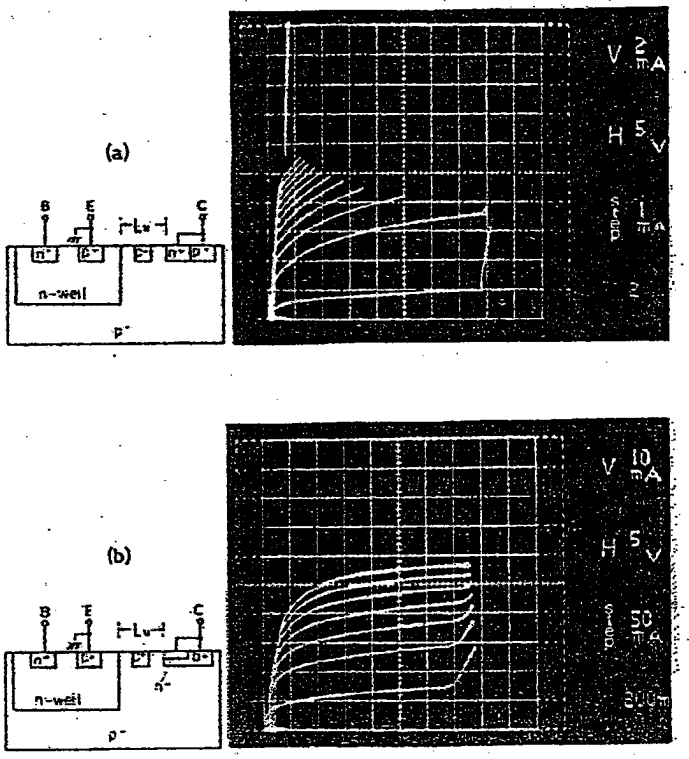

Fig.6 Base noise current at latch up. (a) For conventional CMOS. (b) For CMOS with shielded source structure. Conventional CMOS shows latch up at 6 mA base injection current level, 10 V collector-emitter bias voltage, whereas CMOS with shielded source structure doesn't show latch up phenomena, even at 350-400 mA.

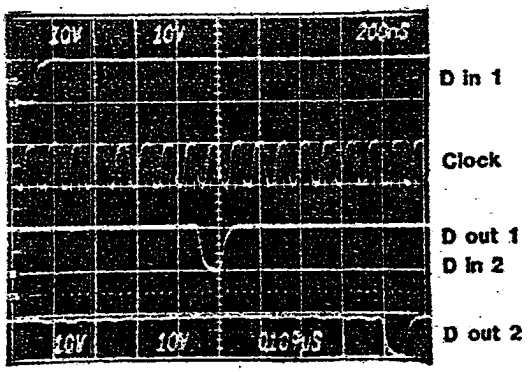

Fig.5 16 stage shift register's input and output waveforms at 9 MHz clock frequency, 10 V. Shift registers operate up to 12 MHz, at 20 V.

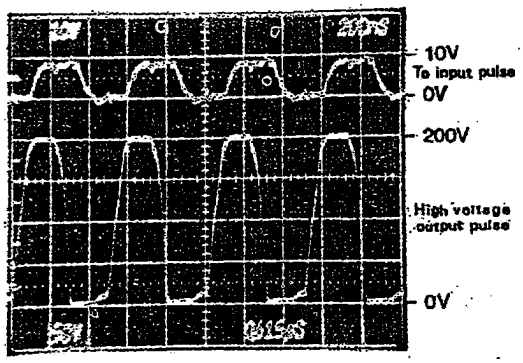

Fig.7 High voltage output waveform, when plasma display panel is driven by the 16 output high voltage MOS IC at 200 V, 2 MHz.

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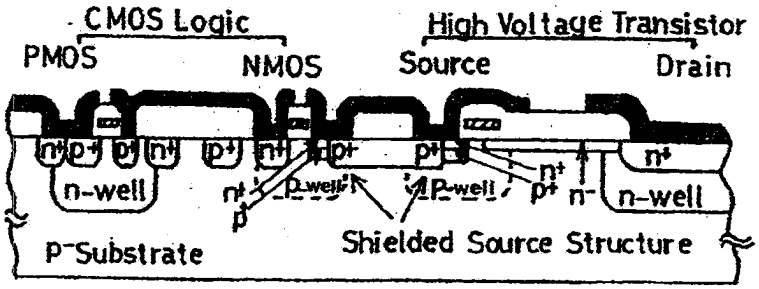
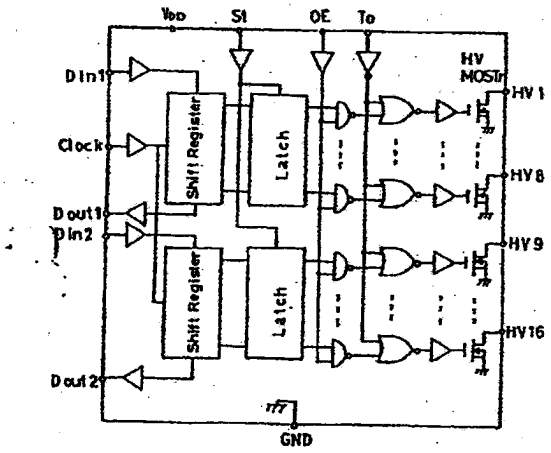


Fig.1 Cross sectional view of high voltage MOS IC with low voltage CMOS logic circuit. Both high and low voltage NMOS transistors have shielded source structure consisting of an upper n^+ source layer entirely shielded by a lower p^+ ground layer.



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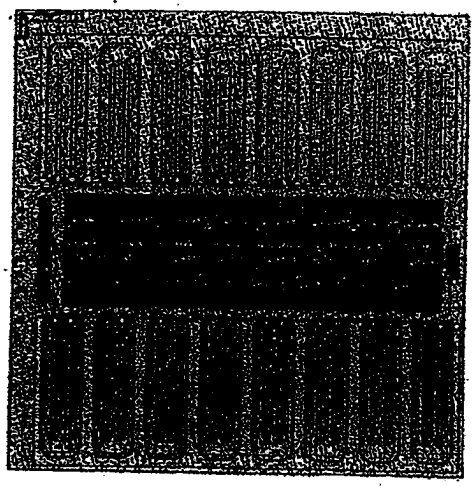

Fig.3 16 output high voltage MOS IC photomicrograph. Chip size is 6 mm x 6 mm.

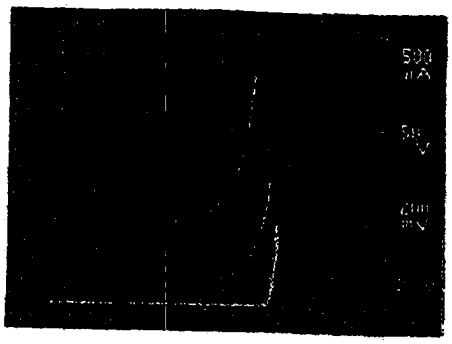

Fig.4 I-V characteristic for high voltage NMOS transistor with shielded source structure, which shows about 400 V drain breakdown voltage.

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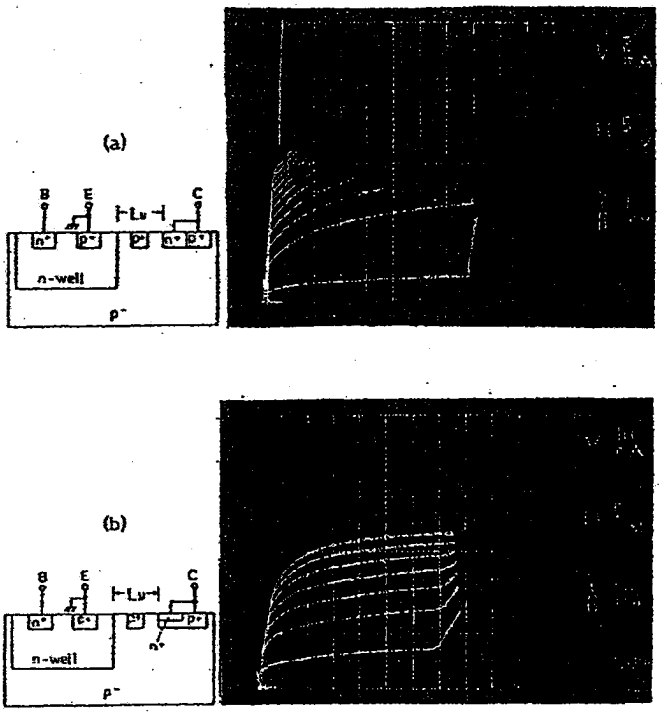

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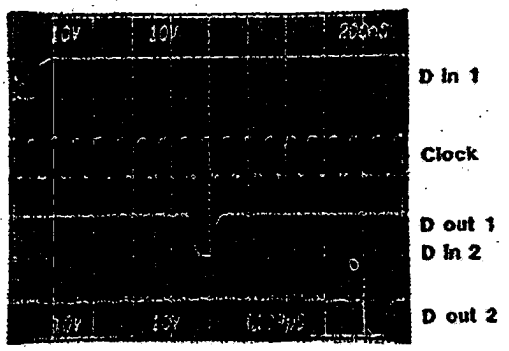


Fig.5 16 stage shift register's input and output waveforms at 9 MHz clock frequency, 10 V. Shift registers operate up to 12 MHz, at 20 V.

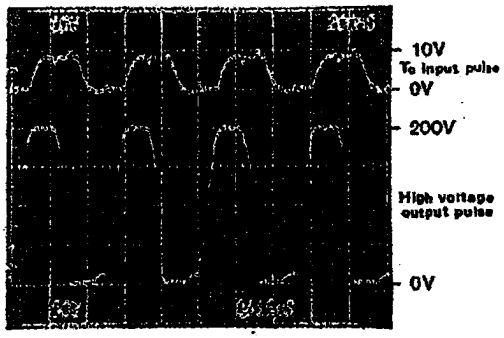
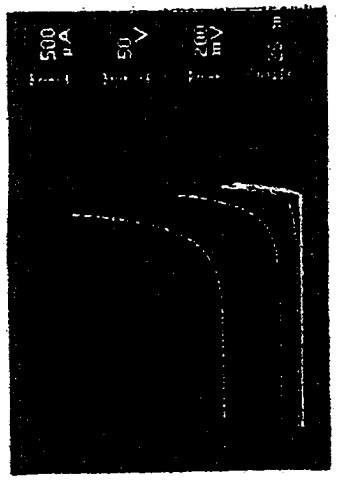
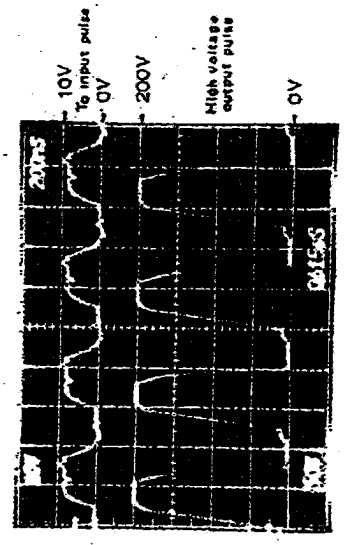


Fig.7 High voltage output waveform, when plasma display panel is driven by the 16 output high voltage MOS IC at 200 V, 2 MHz.


500 µA
50 V
200 mV



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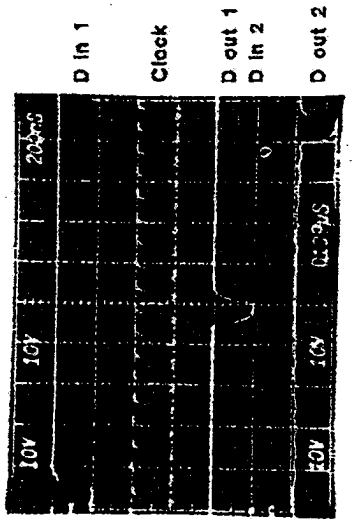

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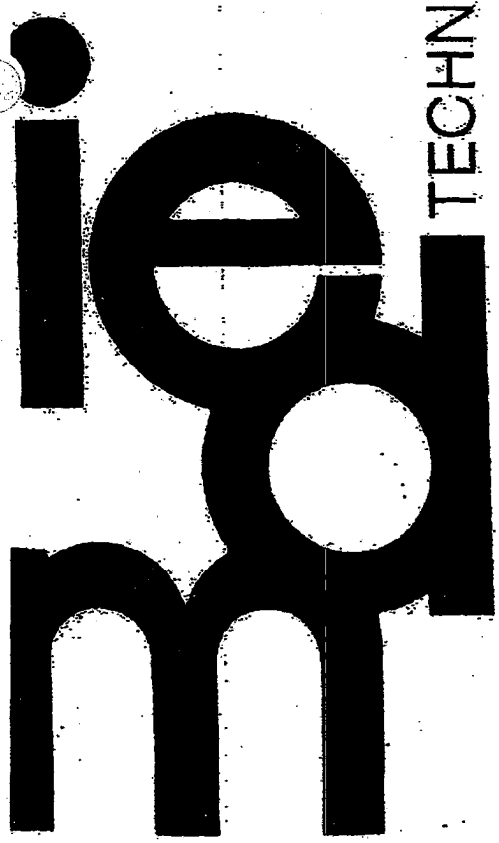

Late News!
Page 785

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1982 International Electron Devices Meeting

TECHNICAL DIGEST

International Electron Devices Meeting.
International Electron Devices Meeting; Technical program.
New York, Institute of Electrical and Electronics Engineers.
v. illus. 23 cm. annual.
Meetings for sponsored by the IEEE Electron Devices Group.
Includes supplements.
1. Electronic apparatus and appliances—Congresses. I. Institute of Electrical and Electronics Engineers. II. Institute of Electrical and Electronics Engineers. Electron Devices Group.
TK7801.I53 621.381'028 78-20188
Library of Congress rev
TT [7202]

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WELCOMING STATEMENT FROM THE GENERAL CHAIRMAN

Al F. Tasch, Jr.
General Chairman

Michael Adler
Technical Program
Chairman

Welcome to the 1982 International Electron Devices Meeting, the international forum for the presentation of latest results of research and development in electron devices! For the first time this meeting is being held in San Francisco in response to the growing geographical base of IEDM participation. In the future the location of the IEDM will alternate between Washington, D.C. and San Francisco.

This meeting, in its 28th year, has and continues to reflect the dramatic growth and pervasiveness of a broad spectrum of electron devices. It has provided the setting for both the exchange and birth of new ideas fueling electronics progress. Both the technical and the international breadth of this conference are evidenced by the program this year which contains 188 contributed papers selected from the 425 submitted abstracts from 17 countries around the world. These papers comprise 29 sessions in six major categories: Solid State Devices; Detectors, Sensors, and Displays; Quantum Electronics and Energy Conversion Devices; Device Technology; Integrated Circuits; and Electron Tubes. In addition, the three areas of Device Technologies for High Speed Logic, Integrated Power Devices, and Automation in Semiconductor Fabrication, are highlighted in the Plenary Session. These areas are further examined in four concurrent panel sessions Tuesday evening which cover: Bipolar and MOS Technology: Choices for VLSI Applications; the Silicon Foundry: Myth or Reality; High Voltage Integrated Circuits: Applications and Technology; and High-Speed Devices and Technology.

An emerging development made possible by the broad electronics progress in the last quarter century, and destined to have a major impact on our society, is the use of robots. The robotics revolution will be addressed by our Tuesday luncheon speaker, Dr. David Nitzan, Director of Robotics Development at SRI International.

I congratulate the Conference Committee for the outstanding job they have done in planning and organizing the 1982 IEDM, and on behalf of the IEEE Electron Devices Society, which sponsors the IEDM, I want to extend my sincere appreciation for their dedicated professional efforts. In addition, the authors are to be commended for their efforts towards technical excellence in their papers. It is with pleasure that I welcome them and all attendees to the 1982 International Electron Devices Meeting.

Al Tasch
General Chairman

TABLE OF CONTENTS

SESSION 20: Evening Panel Discussion 539

Tuesday, December 14, 8:00-10:00 p.m.
Continental Ballrooms 1,2,3,4

Panel Organizer: Joseph C. Logue
IBM
Yorktown Heights, New York

THE SILICON FOUNDRY—MYTH OR REALITY?

PANEL DISCUSSION MEMBERS

Panel Moderator: Joseph C. Logue
IBM
Yorktown Heights, New York

Allan Bell
Xerox
Palo Alto, CA

Dennis Buss
Texas Instruments
Dallas, Texas

Danny Cohen
Cal Tech
Marina Del Rey, CA

Robert Crosby
IBM
Poughkeepsie, NY

Peter Jones
Intel
Chandler, Arizona

Paul Low
IBM
Hopewell Junction, NY

James Meindl
Stanford University
Stanford, CA

Gene Strull
Westinghouse
Baltimore, Maryland

SESSION 21: Evening Panel Discussion 541

Tuesday, December 14, 8:00-10:00 p.m.
Continental Ballroom 5

Panel Organizer: Adrian Hartman
Bell Laboratories
Murray Hill, New Jersey

HIGH VOLTAGE INTEGRATED CIRCUITS—APPLICATIONS AND TECHNOLOGY

PANEL DISCUSSION MEMBERS

Panel Moderator: Adrian R. Hartman
Bell Laboratories
Murray Hill, NJ

Tom Engibous
Texas Instruments
Dallas, TX

Bernd Hoefflinger
Univ. of Minnesota
Minneapolis, MN

Keisuke Kataoka
ORI Electric Industry Co.
Tokyo, Japan

James Mayfield
Sprague Electric Co.
Worcester, MA

Ram Ronen
Xerox Corp.
El Segundo, CA

Ray Roop
Motorola Inc.
Phoenix, AZ

Peter Shackle
Harris Semiconductor
Melbourne, FL

SESSION 22: Evening Panel Discussion 543

Tuesday, December 14, 8:00-10:00 p.m.
Continental Ballroom 6

Panel Organizer: Richard Eden
GigaBit Logic, Inc.
Culver City, California

HIGH-SPEED DEVICES AND TECHNOLOGY

PANEL DISCUSSION MEMBERS

Panel Moderator: Richard C. Eden
GigaBit Logic, Inc.
Culver City, CA

Lester Eastman
Cornell University
Ithica, NY

Herber Kroemer
University of California
Santa Barbara, CA

R. Allen Murphy
MIT Lincoln Laboratories
Lexington, MA

Tushar R. Gheewala
IBM
Yorktown Heights, NY

Nuyen T. Linh
Thompson-CSF
Orsay, France

Paul Solomon
IBM
Yorktown Heights, NY

SESSION 23: Evening Panel Discussion 545

Tuesday, December 14, 8:00-10:00 p.m.
Imperial Room

Panel Organizer: Rick Davies
Texas Instruments
Dallas, Texas

BIPOLAR AND MOS TECHNOLOGY: CHOICES FOR VLSI APPLICATIONS

Panel:

Akio Anzai
Hitachi Ltd.

Harry Boll
Bell Laboratories

Pallab Chatterjee
Texas Instruments

Barry Dunbridge
TRW

Bill Herndon
Fairchild Semiconductor

F.M. Klaassen
Phillips Research, Holland

Tak Ning
IBM

Jim Plummer
Stanford University

HIGH-VOLTAGE DMOS AND PMOS IN ANALOG IC'S

A.W. Ludikhuize

Philips Research Laboratories
Eindhoven - The Netherlands

ABSTRACT

A lateral 300V DMOS device is described which can be integrated in a standard bipolar IC process. The device, applicable as a high voltage source follower for analog circuits, is based upon the "double-acting resurf" principle; a modification with an interrupted p- top layer or with a stepped field plate is used. The p- layer improves the interconnection-induced breakdown and can be used in the extended drain of a 280 V PMOST.

INTRODUCTION

For functions like driving transducers or CRT's and for analog switches, high voltage analog stages of over 250 V may be needed on the chip. Vertical bipolars are less suitable because of the required thick epi-layers and even integration of vertical DMOS devices in a standard IC process is rather difficult. High voltage lateral MOS devices of over 500 V, using thin layer extended drain or "resurf" techniques (1-3), can easily be incorporated, but a high voltage source follower is impossible. Source followers using lateral DMOS devices and 25-30 µm epi have been reported (4); here 200 V is considered the limit for junction isolated devices because of deep isolation diffusions and parasitic bulk and surface effects (5). Recently a "double-acting resurf" technique has been reported (6); compared to "resurf" as mentioned above, it not only offers better lateral conduction but also prevention of substrate punch-through in follower applications. Owing to a higher doping content of the n layer (about 2.10^{12} cm^{-2}), the depletion layer at source (back gate)-to-substrate breakdown does not extend to the surface diffusion (as shown by the left-hand shaded area in fig. 1) and no punch-through occurs. At high voltage on the n$^+$ drain with the other terminals grounded, a high field would occur at the source edge. By using a p-top layer, depletion of the n layer is obtained from the top and the bottom (right-hand shaded areas in fig. 1) causing a smooth voltage decrease over the lateral distance between source and drain; at high drain voltage this p- top layer has to be depleted too. The effect was demonstrated on JFET and lateral bipolar devices (6); the p^- and n layers were optimized at 0.5 10^{12} cm^{-2} and 1.8 10^{12} cm^{-2} respectively.

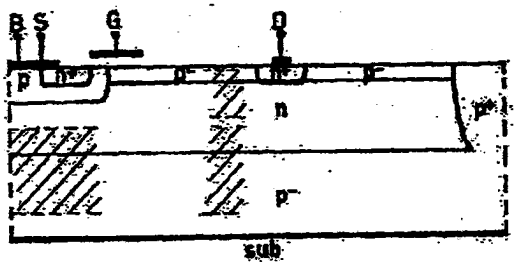

Fig.1. A double-acting resurf structure.

LATERAL DMOST

For proper functioning of a lateral DMOST (LDMOST), the design of fig. 1 has to be adapted. In fig. 2 a window is shown, made locally in the p-layer at the source side; electrons from the gate-controlled surface channel now pass through a vertical JFET which limits the current capability and increases the on-resistance. The window dimensions are therefore a compromise between on-resistance and breakdown.

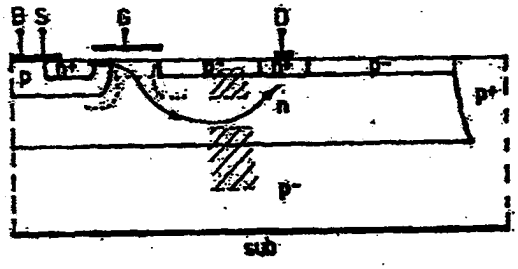

Fig.2. LDMOST with interrupted p-layer.

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Instead of a p-top layer also a stepped field plate, connected to gate or source, can be applied in order to obtain depletion from the surface, as shown in fig. 3.

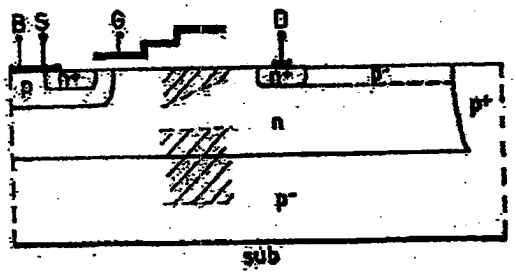

Fig.3. LDMOST with stepped field plate.

The pinching effect on the n layer is much less, lowering the breakdown voltage, but now the entire epi-layer with local accumulation contributes to a low on-resistance.

Computer calculations using our 2D Poisson program "Semmy" were performed on the structure depicted in fig. 4 for several combinations of p-layer and field plates, cf. table 1. A 19 μm 5Ωcm n-type epi-layer as used in a 50-60 V standard bipolar process is applied on a 30Ωcm p-substrate. The 3 μm p-layer, assumed without a window here, has a net dose of $1.6\ 10^{12}$ cm^{-2}; this high value improves the current capability of an extended drain PMOST as will be discussed later on,

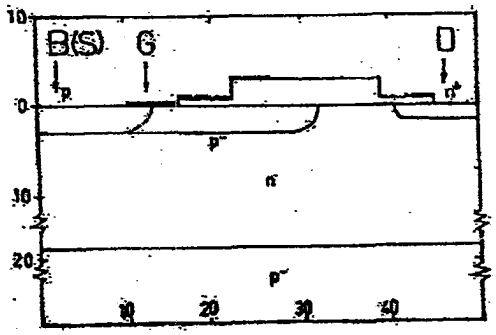

Fig.4. LDMOST structure; dimensions in μm.

but delays pinch off and requires the p-layer to be withdrawn from the n^+ drain in order to prevent low breakdown values. The gate-oxide is 0.1 μm; the field plates (dashed) step on 0.8 and 3.0 μm oxide. The punchthrough voltage to the substrate is calculated to be 600V; spreading of epi dope and thickness may decrease this value to 300 V.

In figs. 5 and 6 equipotential and equifield lines at 300 V drain voltage are shown for a device with a p-layer; the co-operation of top and bottom depletion is visible on the left in fig. 5. The highest field of 23.2 V/μm, obtained at the p-diffusion curvature, does not cause breakdown (avalanche integral <1).

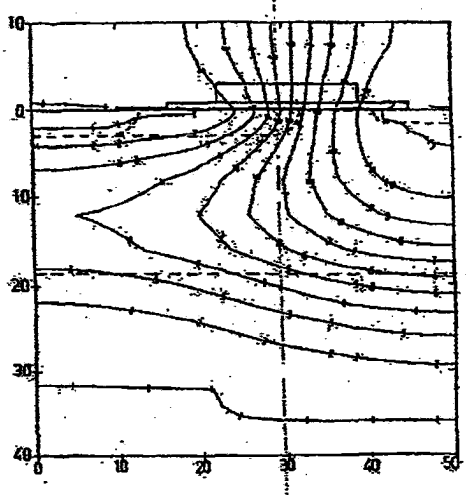

Fig.5. LDMOST equipotential lines at V d-s = 300V; per step 30V, step 1=0V.

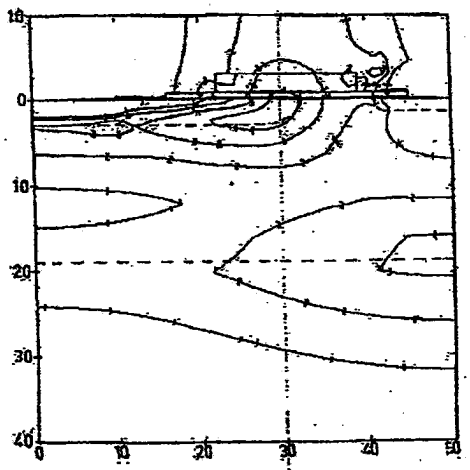

Fig.6. LDMOST equifield lines at V d-s = 300V; per step 5V/μm, step 1=5V/μm.

Table 1 E max (in V/μm) at V d-s=300V; epi, p-layer and field plates (F.P.) as in fig. 4.

substr.	p-	F.P.	E_{maxSi}	B.V.	E_{maxox}
n	yes	yes	32.0	<300	56
p-	no	no	63.5	<<300	177
p-	yes	no	23.2	>300	22.7
p-	no	yes	28.7	>300	95
p-	yes	yes	24.5	>300	35

Fig.7. shows an actual device with a stepped field plate connected to the source; the layout corners are bevelled.
At the connection of the polysilicon gate th e field plate had to be interrupted as single-layer metallization is used and a local p-layer is applied. The active gate width is 500 µm, the channel length is approx. 2.0 µm. The drain surrounds the back gate and prevents parasitic PMOS action from back gate to isolation when the source is at high voltage. As crossing interconnection over shallow n^+ shows only 200V breakdown on 3.0 µm oxide, the shallow n^+ drain has been locally omitted underneath this metallization. A collector wall diffusion

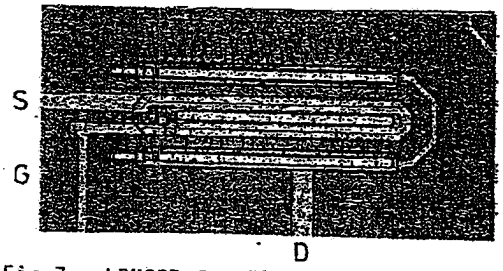

Fig.7. LDMOST for 300V; gate and source with field plate in the centre, n^+ drain 3/4 around as a stopper; drain pitch 90 µm.

or a buried polysilicon field shield can be used here; this way a breakdown >300 V is obtained. At the isolation diffusion edge a p-layer is applied (withdrawn from the n^+ drain), which improves breakdown noticeably in the case of crossing (drain) interconnection and avoids walk-out phenomena below 300V.

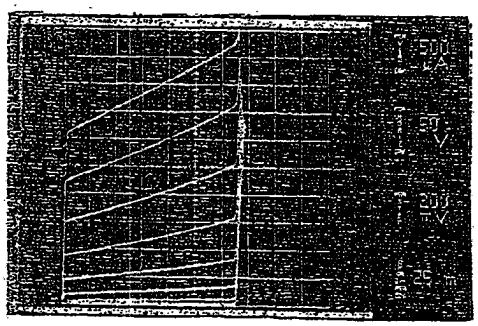

Fig.8. LDMOST BV drain-to-source; the substrate is connected to the source.

A source-to-substrate breakdown of over 300V was obtained limited by the drain-to-isolation distance. Drain-to-source breakdown (substrate is at source potential) is shown in fig. 8 to be over 300V; breakdown generally occurs at the bevelled back gate corners.

Fig. 9 shows the low-voltage on-characteristics. V_T is about 2.4V and β_o =16 µA/V^2; R_{on} is 300 Ω corresponding with 6.7 Ω-mm^2 for the active area. Owing to partial depletion of the epi-layer, R_{on} increases at 300 V s-sub to 450 Ω and I_{max} (10V d-s) becomes 18mA. For a variant according to fig. 2 with a p-ring and 10 µm local windows R_{on} was found to be 450-600 Ω.

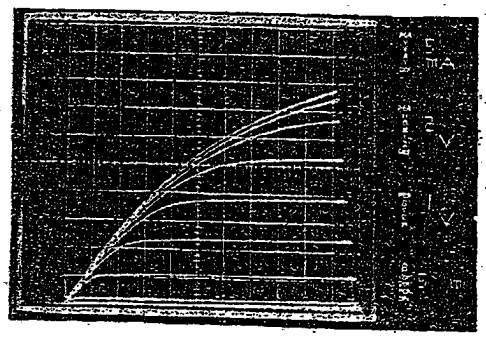

Fig.9. LDMOS on-characteristics.

Experiments in plastic encapsulation showed good stability in dry ambient at 150°C. In wet ambient instabilities are sometimes observed at the drain. Simulation with a field plate at V_{surf} on 1 µm nitride on top of the structure indicated the drain configuration of fig. 4 to be poor; a field plate overlapping the n^+ drain edge is sufficient.

EXTENDED DRAIN PMOST

In the same process a complementary high-voltage extended drain PMOST (EPMOST) has been made; the extension is pinched between the epi-layer and a stepped field plate connected to source or gate (cf. ref.7). For better gradual pinching and less Early effect in the PMOS channel, a buried n^+ layer is applied locally as shown in fig. 10. Source and back gate are

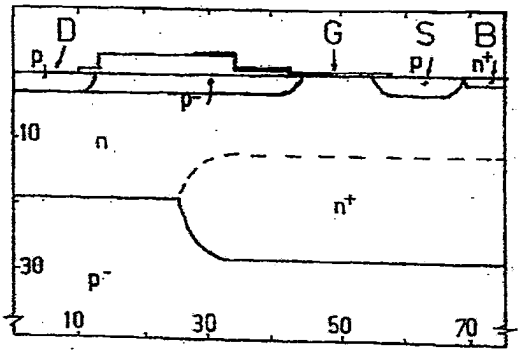

Fig.10. Extended drain PMOST structure.

situated on the right, drain and p- extension on the left. The effective channel length is about 11 µm, but lower values with more Early-effect are possible. A computer calculation with 300V on source and gate shows equipotential and equifield lines (figs. 11 and 12); the maximum field of 23V/µm does not cause breakdown. An actual EPMOST is shown in fig. 13; the p drain is in the centre and the n^+ backgate contact on the outside of the device acts as a stopper for parasitic PMOS action.

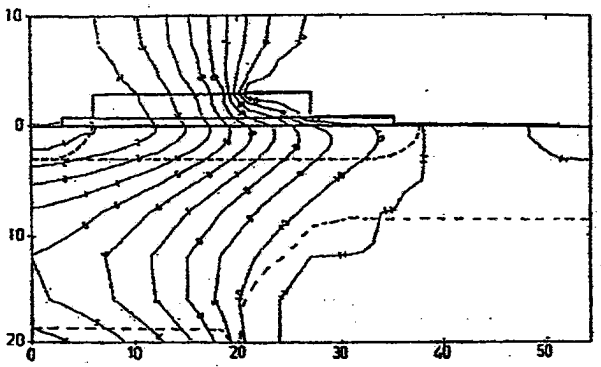

Fig.11. EPMOST equipotential lines at V s, g-d, sub=300V; per step 30V, step 1=0V.

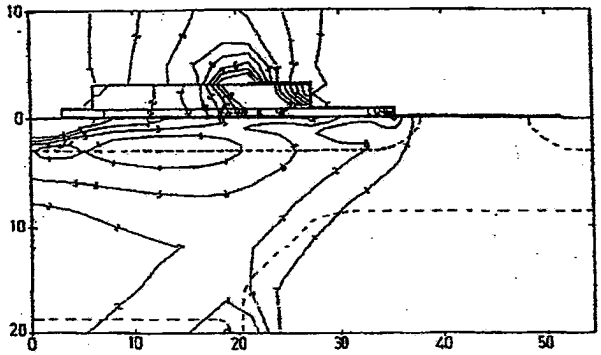

Fig.12. EPMOST equifield lines at V s, g-d, sub=300V; per step 5V/µm, step 1=5V/µm.

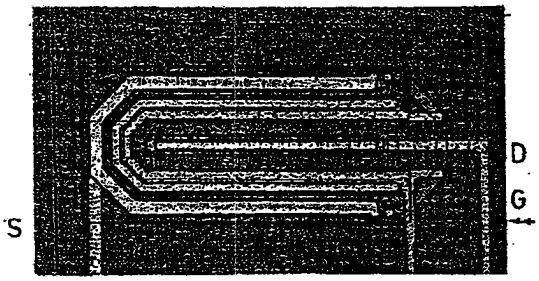

Fig.13. EPMOST with central drain and gate, source and back gate 3/4 around; the n^+ back gate acts as a stopper; scale as fig. 7.

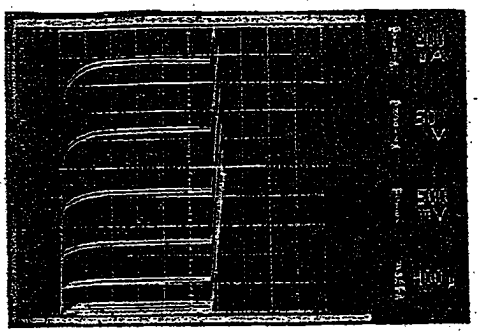

Fig.14. EPMOST BV drain-to-source; the substrate is connected to the drain.

The measured drain-to-source breakdown is shown in fig. 14 to be 280V; this breakdown occurs at the small-radius end of the drain. The active gate width is about 550 µm; V_T=1.5V, g_m max ($10V_{d-s}$)=1.4mA/V and β_o=7µA/V^2.R_{on} is 900 Ω, corresponding with 30Ωmm for the active area.

CONCLUSION

By using a modification of the "double-acting resurf" principle, a lateral DMOST for 300V analog applications can be integrated with standard bipolar components. The use of a p- implanted layer allows interconnections to over 300V on 3 µm oxide. The same p-layer has been used in an extended drain PMOST of 280V.

ACKNOWLEDGEMENT

The author wishes to thank his colleagues for their stimulating co-operation and particularly W. Ruis and R. Bonne for preparation of the samples.

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